

APPLICATION DATA SHEET

Electronic Version v14

Stylesheet Version v14.0

Title of Invention	METHOD FOR SEPARATELY OPTIMIZING THIN GATE DIELECTRIC OF PMOS AND NMOS TRANSISTORS WITHIN THE SAME SEMICONDUCTOR CHIP AND DEVICE MANUFACTURED THEREBY
Application Type :	regular, utility
Attorney Docket Number :	FIS920030228US1
Correspondence address:	
Customer Number:	32074
	
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Publication Information:
Suggested Figure for Publication - 1
Suggested Classification -
Suggested Technology Center -
Total Number of Drawing Sheets - 17

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